AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-4 (Canceled without prejudice or disclaimer).

5. (Original) A method of manufacturing a semiconductor integrated circuit device having a plurality of wiring layers and including a first wiring layer which is not the uppermost layer among said plurality of wiring layers and a second wiring layer higher than said first wiring layer in said plurality of wiring layers, comprising:

(a) a step of depositing a first insulating film, a second insulating film, and a third insulating film in order on said first wiring layer;

(b) a step of patterning a first mask film having an opening in an area in which holes will be formed on said third insulating film and etching said third insulating film under presence of said first mask film;

(c) a step of removing said first mask film and depositing a fourth insulating film and a fifth insulating film in order on said third and second insulating films;

(d) a step of patterning a second mask film having an opening in an area in which trenches will be formed on said fifth insulating film and etching said fifth insulating film under presence of said second mask film;

(e) a step of etching said fourth insulating film by using the second mask film or said fifth insulating film as a mask, forming the trenches patterned on said fifth

insulating film on said fourth insulating film, etching said second insulating film by using said third insulating film as a mask, and forming the holes patterned on said insulating film on said second insulating film;

(f) a step of removing said third insulating film and said first insulating film exposed to bottoms of said trenches and holes;

(g) a step of depositing a sixth insulating film on the entire surface of a semiconductor substrate including insides of said trenches and holes;

(h) a step of patterning a third mask film for covering at least some of said holes;

(i) a step of etching said sixth insulating film under presence of said third mask film;

(j) a step of removing said third mask film and forming a conductive film for filling up said trenches and holes; and

(k) a step of removing said conductive film from areas other than said trenches and forming wirings comprising said second wiring layer and a conductive member.

8. (Original) A method of manufacturing a semiconductor integrated circuit device having a plurality of wiring layers and including a first wiring layer which is not the uppermost layer among said plurality of wiring layers and a second wiring layer higher than said first wiring layer in said plurality of wiring layers, comprising:

(a) a step of depositing a first insulating film, a second insulating film, and a third insulating film in order on said first wiring layer;

(b) a step of patterning a first mask film having an opening in an area in which holes will be formed on said third insulating film and etching said third insulating film under presence of said first mask film;

(c) a step of removing said first mask film and depositing a fourth insulating film and a fifth insulating film in order on said third and second insulating films;

(d) a step of patterning a second mask film having an opening in an area in which trenches will be formed on said fifth insulating film and etching said fifth insulating film under presence of said second mask film;

(e) a step of etching said fourth insulating film by using the second mask film or said fifth insulating film as a mask, forming the trenches patterned on said fifth insulating film on said fourth insulating film, etching said second insulating film by using said third insulating film as a mask, and forming the holes patterned on said insulating film on said second insulating film;

(f) a step of patterning a third mask film for covering at least some of said holes;

(g) a step of etching said first insulating film at bottoms of said holes and said third insulating film at bottoms of said trenches under presence of the third mask film and patterned fifth insulating film;

(h) a step of removing said third mask film and forming a conductive film for filling up said trenches and holes; and

(i) a step of removing said conductive film from areas other than said trenches and forming wirings for comprising said second wiring layer and a conductive member.

18. (Original) A method of manufacturing a semiconductor integrated circuit device having a plurality of wiring layers and including a first wiring layer which is not the uppermost layer among said plurality of wiring layers and a second wiring layer higher than said first wiring layer in said plurality of wiring layers, comprising:

(a) a step of depositing a first insulating film, a second insulating film, a third insulating film, a fourth insulating film, and a fifth insulating film in order on said first wiring layer;

(b) a step of pattering a first mask film having an opening in an area in which holes will be formed on said fifth insulating film, etching said fifth, fourth, third, and second insulating films under presence of said first mask film, and forming holes;

(c) a step of removing said first mask film, forming a second mask film on said fifth insulating film, exposing an area in which trenches will be formed, developing said second mask film, and leaving said mask film in areas other than the area in which said trenches will be formed and in said holes;

(d) a step of etching said fifth and the fourth insulating film and forming trenches presence of the second mask film;

(e) a step of removing said second mask film and patterning a third mask film for covering at least some of said holes;

(f) a step of etching said first insulating film at the bottoms of said holes under presence of said third mask film;

(g) a step of removing said third mask film and forming a conductive film for filling up said trenches and holes; and

(h) a step of removing said conductive film in areas other than said trenches and forming wiring comprising said second wiring layer and a conductive member.

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8. (Original) A method of manufacturing a semiconductor integrated circuit device according to claim 6, further comprising a step of depositing a sixth insulating film on the entire surface of a semiconductor substrate including insides of said trenches and holes before forming said third mask film, wherein said sixth insulating film not covered with said third mask film is removed together with said first insulating film in the step of etching said first insulating film at bottoms of said holes.

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9. (Original) A method of manufacturing a semiconductor integrated circuit device according to claim 7, further comprising a step of depositing a sixth insulating film on the entire surface of a semiconductor substrate including insides of said trenches and holes before forming said third mask film, wherein said sixth insulating film not covered with said third mask film is removed together with said first insulating film in the step of etching said first insulating film at bottoms of said holes.

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10. (Original) A method of manufacturing a semiconductor integrated circuit device having a plurality of wiring layers and including a first wiring layer which is not the uppermost layer among said plurality of wiring layers and a second wiring layer higher than said first wiring layer in said plurality of wiring layers, comprising:

(a) a step of depositing a seventh insulating film for covering said first wiring layer;

(b) a step of patterning a first mask film having an opening in an area in which holes will be formed on said seventh insulating film, etching said seventh insulating film under presence of said first mask film, and removing said seventh insulating film onto wirings comprising said first wiring layer;

(c) a step of depositing a sixth insulating film on the entire surface of a semiconductor substrate including insides of said holes;

(d) a step of pattering a third mask film for covering at least some of said holes;

(e) a step of etching said sixth insulating film under presence of said third mask film;

(f) a step of removing said third mask film and forming a conductive film for filling up said holes;

(g) a step of removing said conductive film from areas other than said holes and forming a conductive member to be connected to wirings comprising said second wiring layer; and

(h) a step of depositing a second conductive film on the entire surface of said semiconductor substrate, patterning said second conductive film, and forming said second wiring layer.

11. (Original) A method of manufacturing a semiconductor integrated circuit device manufacturing method according to claim 5, wherein:

said first and third insulating films are formed of a material having an etching selection ratio to said second and fourth insulating films and the thickness of said first insulating film is equal to that of said third insulating film.

12. (Original) A method of manufacturing a semiconductor integrated circuit device manufacturing method according to claim 6, wherein:

said first and third insulating films are formed of a material having an etching selection ratio to said second and fourth insulating films and the thickness of said first insulating film is equal to that of said third insulating film.

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~~13.~~ (Original) A method of manufacturing a semiconductor integrated circuit device manufacturing method according to claim 7, wherein:

said first and third insulating films are formed of a material having an etching selection ratio to said second and fourth insulating films and the thickness of said first insulating film is equal to that of said third insulating film.

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~~14.~~ (Original) A method of manufacturing a semiconductor integrated circuit device manufacturing method according to claim 8, wherein:

said first and third insulating films are formed of a material having an etching selection ratio to said second and fourth insulating films and the thickness of said first insulating film is equal to that of said third insulating film.

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~~15.~~ (Original) A method of manufacturing a semiconductor integrated circuit device manufacturing method according to claim 9, wherein:

said first and third insulating films are formed of a material having an etching selection ratio to said second and fourth insulating films and the thickness of said first insulating film is equal to that of said third insulating film.

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~~16.~~ (Original) A method of manufacturing a semiconductor integrated circuit device manufacturing method according to claim 10, wherein:

said first and third insulating films are formed of a material having an etching selection ratio to said second and fourth insulating films and the thickness of said first insulating film is equal to that of said third insulating film.

17. (Original) A method of manufacturing a semiconductor device according to claim 5, wherein the thickness of said first or sixth insulating film is smaller than that of said second insulating film.

18. (Original) A method of manufacturing a semiconductor device according to claim 8, wherein the thickness of said first or sixth insulating film is smaller than that of said second insulating film.

19. (Original) A method of manufacturing a semiconductor device according to claim 7, wherein the thickness of said first or sixth insulating film is smaller than that of said second insulating film.

20. (Original) A method of manufacturing a semiconductor device according to claim 8, wherein the thickness of said first or sixth insulating film is smaller than that of said second insulating film.

21. (Original) A method of manufacturing a semiconductor device according to claim 8, wherein the thickness of said first or sixth insulating film is smaller than that of said second insulating film.

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22. (Original) A method of manufacturing a semiconductor device according to claim 10, wherein the thickness of said first or sixth insulating film is smaller than that of said second insulating film.

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23. (Original) A method of manufacturing a semiconductor device according to claim 11, wherein the thickness of said first or sixth insulating film is smaller than that of said second insulating film.

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24. (Original) A method of manufacturing a semiconductor device according to claim 12, wherein the thickness of said first or sixth insulating film is smaller than that of said second insulating film.

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25. (Original) A method of manufacturing a semiconductor device according to claim 13, wherein the thickness of said first or sixth insulating film is smaller than that of said second insulating film.

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26. (Original) A method of manufacturing a semiconductor device according to claim 14, wherein the thickness of said first or sixth insulating film is smaller than that of said second insulating film.

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27. (Original) A method of manufacturing a semiconductor device according to claim 15, wherein the thickness of said first or sixth insulating film is smaller than that of said second insulating film.

28. (Original) A method of manufacturing a semiconductor device according to claim 16, wherein the thickness of said first or sixth insulating film is smaller than that of said second insulating film.

29. (Original) The semiconductor integrated circuit device manufacturing method according to claim 5, wherein the permittivity of said first or sixth insulating film is higher than that of said second insulating film.

30. (Original) The semiconductor integrated circuit device manufacturing method according to claim 6, wherein the permittivity of said first or sixth insulating film is higher than that of said second insulating film.

31. (Original) The semiconductor integrated circuit device manufacturing method according to claim 7, wherein the permittivity of said first or sixth insulating film is higher than that of said second insulating film.

32. (Original) The semiconductor integrated circuit device manufacturing method according to claim 8, wherein the permittivity of said first or sixth insulating film is higher than that of said second insulating film.

33. (Original) The semiconductor integrated circuit device manufacturing method according to claim 9, wherein the permittivity of said first or sixth insulating film is higher than that of said second insulating film.

34. (Original) The semiconductor integrated circuit device manufacturing method according to claim 28, wherein the permittivity of said first or sixth insulating film is higher than that of said second insulating film.

35. (Original) The semiconductor integrated circuit device manufacturing method according to claim 1, wherein the permittivity of said first or sixth insulating film is higher than that of said second insulating film.

36. (Original) The semiconductor integrated circuit device manufacturing method according to claim 3, wherein the permittivity of said first or sixth insulating film is higher than that of said second insulating film.

37. (Original) A method of generating a mask-pattern used for a method of manufacturing a semiconductor integrated circuit device having a plurality of wiring layers and including a first wiring layer which is not the uppermost layer among said plurality of wiring layers and a second wiring layer higher than said first wiring layer in said plurality of wiring layers, comprising:

(a) a first step of determining an intersectional area where a first power-source wiring to which a first potential is assigned among power-source wiring comprising said wiring layer intersects a second power-source wiring to which a second potential different from said first potential is assigned among power-source wiring comprising said second wiring layer;

a second step of generating a hole pattern in said intersectional area; and

a third step of expanding the width of said hole pattern so as not to reach wiring areas of said first and second wiring layers adjacent to said hole pattern.

38. (New) The method of generating a mask-pattern according to claim 37, wherein said semiconductor integrated circuit device has a capacitive element in said intersectional area between said first power-source wiring and said second power-source wiring.

39. (New) The method of generating a mask-pattern according to claim 38, further comprising:

a fourth step of generating a mask-pattern for said first wiring layer by synthesizing a wiring pattern of said first wiring layer and said hole pattern and generating a mask-pattern for said second wiring layer by synthesizing a wiring pattern of said second wiring layer and said hole pattern.

40. (New) The method of generating a mask-pattern according to claim 38, wherein said third step includes expanding the area of the hole pattern for the capacitive element.

41. (New) A method of generating a mask-pattern according to claim 40, wherein a fourth step of generating a mask-pattern for said first wiring layer by synthesizing a wiring pattern of said first wiring layer and said hole pattern and generating a mask-pattern for said second wiring layer by synthesizing a wiring pattern of said second wiring layer and said hole pattern.